What is Claimed is:

1. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of look-up table based logic elements, the method comprising:

evaluating whether a first look-up table based logic element can be configured in a way to utilize less power taking into account at least one of embedded drivers, differing transistor types, and differing transistor sizings; and

if the first look-up table based logic element is configured to utilize minimum power, then proceeding to evaluate a second look-up table based logic element; and

if the first look-up table based logic element is not configured to utilize minimum power, then rotating the inputs of the first look-up table based logic element such that the pass transistors associated with the first look-up table based logic element consume a minimum power.

2. The method of claim 1, wherein the evaluating occurs during a technology mapping relating to the first look-up table based logic element.

3. The method of claim 1, wherein the evaluating occurs during a routing period relating to the first look-up table based logic element.

4. The method of claim 1, wherein the evaluating occurs following a routing period relating to the first look-up table based logic element.

5. The method of claim 1, further comprising determining the change in speed of a function associated with the first look-up table based logic element, the change in speed that is attributable to the rotation.

6. The method of claim 1, further comprising determining the change in area of the first look-up table based logic element and the associated routing, the change in area that is attributable to the rotation.

7. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of look-up table based logic elements, the method comprising:

evaluating whether a first look-up table based logic element utilizes all of its inputs; and

if the first look-up table based logic element utilizes all of its inputs, then proceeding to evaluate a second look-up table based logic element; and

if the first look-up table based logic element does not utilize all of its inputs, then determining whether, if the inputs of the first element are rotated, any storage locations associated with the unused input are freely configurable; and

if a greater number of the storage locations associated with the first element are freely configurable than before the rotation, then performing the rotation such that the pass transistors associated with the unused input consume a minimum power.

8. The method of claim 7, wherein the evaluating occurs during a technology mapping relating to the first look-up table based logic element.

9. The method of claim 7, wherein the evaluating occurs during a routing period relating to the first look-up table based logic element.

10. The method of claim 7, wherein the evaluating occurs following a routing period relating to the first look-up table based logic element.

11. The method of claim 7, further comprising determining the change in speed of a function associated with the first look-up table based logic element, the change in speed that is attributable to the rotation.

12. The method of claim 7, further comprising determining the change in area of the first look-up table based logic element and the associated routing, the change in area that is attributable to the rotation.

13. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of logic elements, the method comprising:

evaluating whether a first logic element is set to minimize static power consumption;

if the first logic element is set to minimize power consumption, then proceeding to evaluate a second logic element; and

if the first logic element is not set to minimize power consumption and the logic element is freely configurable then configuring the logic element to consume less static power.

14. The method of claim 13, wherein the evaluating occurs during a technology mapping relating to the first logic element.

15. The method of claim 13, wherein the evaluating occurs during a routing period relating to the first logic element.

16. The method of claim 13, wherein the evaluating occurs following a routing period relating to the first logic element.

17. The method of claim 13, further comprising determining the change in speed of a function associated with the first logic element, the change in speed that is attributable to the configuring.

18. The method of claim 13, further comprising determining the change in area of the first logic element and the associated routing, the change in area that is attributable to the configuring.

19. The method of claim 13, wherein the configuring comprising increasing a number of transistors associated with the logic element that have substantially no voltage differential between a source and a drain.

20. The method of claim 13, wherein the increasing comprises rotating the inputs of the logic element.

21. A method for reducing power consumption in a programmable logic device, the programmable logic device being potentially programmed at least in part by a proposed technology mapping, the method comprising:

if an alternative technology mapping exists for the proposed technology mapping then determine the estimated power consumption of each of the possible technology mappings and determine the least power consumptive technology mapping; and

if alternative technology mapping does not exist for the proposed technology mapping then implementing the proposed technology mapping.

22. The method of claim 21, further comprising determining the change in speed of a function associated with the proposed technology mapping, the change in speed that is attributable to the configuring.

23. The method of claim 21, further comprising comparing the area associated with the proposed technology mapping and the area associated with the alternative technology mapping.

24. The method of claim 21, wherein the alternative technology mapping comprises inverting at least one output of the proposed technology mapping.

25. A method for reducing power consumption in a programmable logic device, the programmable logic

device comprising a plurality of look-up tables, the method comprising:

evaluating whether switching frequencies on each of the inputs of a first look-up table are substantially the same;

if one of the inputs of the look-up table has a switching frequency that is relatively higher than the other inputs and the higher frequency input can be rotated to a position where it consumes less power, then rotate the higher frequency input such that the higher frequency input consumes less power; and

if none of the inputs of the look-up table has a switching frequency that is relatively higher than the other inputs, then proceed to evaluate a second look-up table.

26. The method of claim 25, wherein the evaluating occurs during a technology mapping relating to the first look-up table.

27. The method of claim 25, wherein the evaluating occurs during a routing period relating to the first look-up table.

28. The method of claim 25, wherein the evaluating occurs following a routing period relating to the first look-up table.

29. The method of claim 25, further comprising determining the change in speed of a function associated with the first look-up table, the change in speed that is attributable to the rotation.

30. The method of claim 25, further comprising determining the change in area of the first look-up table and the associated routing, the change in area that is attributable to the rotation.

31. The method of claim 25, wherein the rotating the higher frequency input to a position where it consumes less power comprising rotating the input to a position that is more proximal to the output of the look-up table.

32. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of look-up tables, the method comprising:

evaluating whether switching frequencies on each of the inputs of a first function implemented across multiple look-up tables are substantially the same;

if one of the inputs of the multi-look-up table function has a switching frequency that is relatively higher than the other inputs and the higher frequency input can be rotated to a position where it consumes less power, and this movement can be done while complying with area and speed requirements associated with the programmable logic device, then rotate the higher frequency input such that the higher frequency input consumes less power; and

if none of the inputs of the multi-look-up table function has a switching frequency that is relatively higher than the other inputs, then proceed

to evaluate a second function implemented across multiple look-up tables.

33. The method of claim 32, wherein the evaluating occurs during a technology mapping relating to the first function.

34. The method of claim 32, wherein the evaluating occurs during a routing period relating to the first function.

35. The method of claim 32, wherein the evaluating occurs following a routing period relating to the first function.

36. The method of claim 32, further comprising determining a change in speed of the first function, the change in speed that is attributable to the rotation.

37. The method of claim 32, further comprising determining a change in area of the first function, the change in area that is attributable to the rotation.

38. The method of claim 32, wherein the rotating the higher frequency input to a position where it consumes less power comprising rotating the input to a position that is more proximal to the output of the first function.

39. A programmable logic device including a logic element, the logic element comprising a fixed number of transistors that are substantially always OFF in a static state of operation of the logic element, the system configured to:

increase the number of storage locations associated with the transistors that are always OFF while maintaining a system functionality threshold; and

after each storage location is associated with a transistor that is substantially always OFF, minimize the static power by analysis and manipulation of storage locations having don't care status.

40. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of look-up table based logic elements, the method comprising:

evaluating whether a first look-up table based logic element utilizes all of its inputs during the operation of the programmable logic device; and

if the first look-up table based logic element utilizes all of its inputs during the operation of the programmable logic device, then proceeding to evaluate a second look-up table based logic element; and

if the first look-up table based logic element does not utilize all of its inputs for some portion of the operational time of the programmable logic device, then determining whether, if the inputs of the first element that are not utilized for the portion of the operational time of the programmable logic device are rotated, any storage locations associated with the inputs that are not utilized are freely configurable; and

if more of the storage locations associated with the first element are freely configurable than before the rotation, then performing the rotation such that the pass transistors associated with the unused input consume a minimum power.

41. The method of claim 40, wherein the evaluating occurs during a technology mapping relating to the first look-up table based logic element.

42. The method of claim 40, wherein the evaluating occurs during a routing period relating to the first look-up table based logic element.

43. The method of claim 40, wherein the evaluating occurs following a routing period relating to the first look-up table based logic element.

44. The method of claim 40, further comprising determining the change in speed of a function associated with the first look-up table based logic element, the change in speed that is attributable to the rotation.

45. The method of claim 40, further comprising determining the change in area of the first look-up table based logic element and the associated routing, the change in area that is attributable to the rotation.

46. A method for reducing power consumption in a programmable logic device, the programmable logic device comprising a plurality of logic elements, the method comprising:

evaluating whether a first logic element is used during the operation of the programmable logic device;

if the first look-up table based logic element is used during the operation of the programmable logic device, then proceeding to evaluate a second look-up table based logic element;

if the first look-up table based logic element is not used during the operation of the programmable logic device, then determining a minimum power state of the unused logic element; and .

evaluating whether the minimum power output state of the unused logic element should be implemented taking into account at least one of routing and performance of the programmable logic device.

47. The method of claim 46, wherein the evaluating occurs during a technology mapping relating to the first logic element.

48. The method of claim 46, wherein the evaluating occurs during a routing period relating to the first logic element.

49. The method of claim 46, wherein the evaluating occurs following a routing period relating to the first logic element.

50. The method of claim 46, further comprising determining the change in speed of a function associated with the operation of the programmable logic element, the change in speed that is

attributable to the implementation of the minimum power state of the first logic element.